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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,362	02/07/2002	Kuan-Yu Fu	CPH35726-D1	2716

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EXAMINER	
HU, SHOUXIANG	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 07/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,362	FU, KUAN-YU	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/059,548.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 10-15 are objected to because of the following informalities and/or defects:

In claims 10 and 13, the terms of "said first and second trench" should read as: --said first and second trenches--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10-15, as being best understood in view of the claim objections above, are rejected as being unpatentable over Lancaster (US 4,835,584) in view of Lee (US 4,685,196) and/or Solomon (US 5,108,938).

Lancaster discloses a semiconductor structure (Figs. 1-7F, especially Figs. 4, 5L, and/or 7F), comprising a substrate having an active region including a channel region (under each bottom of the gate oxide layer 57 in Figs. 4 and/or 5L or 72 in Fig. 7F) and a non-channel region surrounding the channel region; a first trench and a second trench disposed near the channel region, a thin insulating layer (57 in Figs. 4 and/or 5L or 72 in

Fig. 7F; a silicon oxide gate insulating layer, about 0.1 um, see col. 3, line 61) over the first and second trenches and conformal to the profile of the first and second trenches; a gate electrode (58 in Fig. 5L or 75 in Fig. 7F) disposed over the two trenches and comprising a first vertical portion, a second vertical portion and a horizontal portion (see the interconnection portion in Figs. 4, 5G and 7B above the trenches that connects the two vertical portions of the gate in the neighboring trenches), with the first vertical portion being embedded inside and substantially fills the first trench, the second vertical portion being embedded inside and substantially fills the second trench, and the horizontal portion being disposed over the substrate and connecting the first and second vertical portions together; a first shallow doped region (the top horizontal portion of region 14, 73 or 77) within the substrate at an upper corner adjacent to the first vertical portion of the gate electrode and a second shallow doped region (the upper horizontal portion of region 14, 74 or 78) at an upper corner adjacent to the second vertical portion of the gate electrode; a deep source region (the lower portion of region 14, 73 or 77) and a deep drain region (the lower portion of region 14, 74 or 78) disposed in a region in the substrate at a depth deeper than the first and second trenches.

The insulating layer and the gate electrode in Lancaster can completely fill the trenches along the channel width direction (see Figs. 6 and 7).

Although Lancaster does not expressly disclose that the insulating layer and the gate electrode can also completely fill the trenches along the channel length direction (i.e., the source-to-drain direction, which is perpendicular to the channel width direction), one of ordinary skilled in the art would readily recognize that such complete filling would

be desirable either for enhancing the gate conductance by maximally expanding the gate size along the source-to drain direction while still being insulated from the source and drain regions with the insulating layer, or for minimizing the device size along the source and drain direction by eliminating as many non-active spaces as possible along the source-to-drain direction, as evidenced in Lee (see the gate 24 and the insulating layer 22 in the cover page figure) or in Solomon (see the gate 57 and the insulating layer 61 in the cover page figure).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the device of Lancaster with the gate and the insulating film completely filling the trenches along the source-to-drain direction, per the teachings of Lee and/or Solomon, so that a semiconductor structure with enhanced gate conductance and/or reduced device size would be obtained.

Regarding claims 11 and 14, it is noted that it is art known that the insulating layer used as a gate oxide layer can be readily formed through thermal oxidation for achieving high quality in the gate insulating layer, as further evidenced in Lee (see col. 3, lines 61-66).

Response to Arguments

3. Applicant's arguments filed on January 17, 2006 have been fully considered but they are not persuasive. It is noted that the applied prior art references do teach the claimed invention including the recited horizontal portion, as Lancaster expressly teaches to form a structure with multiplicity of trenched gates for gain advantage (see

col. 2, lines 49-55). In such a multiple-trench gate structure, the vertical gate portions inside the trenches have to be interconnected together with horizontal portion(s) above the level of the trenches, such as with the top horizontal portions of the interconnected gate electrode shown in Fig. 4, or the top horizontal portions of gate layer 58 in Fig. 5G, or the interconnection portion 74 in Fig. 7B, which later merged with vertical gate portions 73 to become interconnected gate electrode 75 in Figs. 7C-7F. Although such vertical gate portions and/or the horizontal interconnection portions may be trimmed along the channel length direction, as shown in Figs. 4, 5L and/or 7F, the remaining vertical gate portions in Lancaster naturally remain to be interconnected through the remaining horizontal portions along the channel width direction (especially see Figs. 4, 5G and/or 7D); otherwise at least some of the vertical gate portions would be left to be unconnected so as to be electrically floating, which would cause the gate structure with the multiple trenched gate portions in Lancaster to be non-operative.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
July 5, 2006

SHOUXIANG HU
PRIMARY EXAMINER